A Second Harmonic Class-F Power Amplifier in Standard CMOS Technology

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***Abstract*—For personal communications systems, the highest possible integration on monolithic technology of all RF functions is desirable. The most difficult component to be monolithically integrated with all other functions is the output power amplifier. This paper describes the design and test of an integrated class-F power amplifier with 200-mW output power at 1.9 GHz and a 3-V power supply based on a 0.6-μm CMOS standard technology. A theoretical study of class-F operation that highlights the influence of nonideal active devices and output network topology on the circuit behavior was performed to have guidelines for amplifier optimization.**

***Index Terms*—Class F, CMOS, power amplifier.**

I. Introduction

Modern mobile communications demand for low-cost low-power consumption and reduced size and weight equipment. An increasingly higher level of integration is needed to meet these requirements, which is easily achievable for digital and low-frequency signal processing, mainly with CMOS technology. However, as the frequency increases, so does the RF designers difficulties, mainly for power-amplifier designs. Low-voltage operation is helpful for digital circuitry reducing its power consumption, but for power amplifiers, low voltages have to be compensated, resorting to high currents in order to meet power specifications.

The power amplifier is a key element in a wireless communication handset due to its large power consumption. Special care must be taken in order to maximize power-added efficiency (PAE). Drain efficiency is improved by overdriving the amplifier, but keeping enough gain; thus, PAE will not be reduced. Using GaAs and related technologies, where active devices present medium to high gain in the low-gigahertz range, PAE is not reduced when compressing amplifier's gain [1]. With the lower gain of silicon devices, it becomes difficult to obtain power amplifiers with high PAE. Nevertheless, CMOS has proven its ability for low-voltage power amplifiers at 850 MHz [2], [3], while at 2 GHz, a BiCMOS power amplifier has been presented [4]. Recently, a 1.9-GHz CMOS power amplifier has been presented, but its operation is strictly for constant envelope modulation schemes [5].

Class F with a single resonator is a commonly used solution for high-frequency power-amplifier design [6]. However, it is not clear if the best solution is second or third harmonic tuning. Assuming an ideal active device, the Raab maximally flat waveforms study [7] shows similar efficiency for a power amplifier when tuning either the second or third harmonic. A simple theoretical study using a GaAs MESFET without any experimental verification showed better performances when tuning the second harmonic [8].

Manuscript received February 1, 2000; revised January 1, 2001. This work was supported by the Fundação para a Ciência e Tecnologia under Contract POCTI/1999/ESE/34074-LDMOSCA.

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Publisher Item Identifier S 0018-9480(01)04444-1.

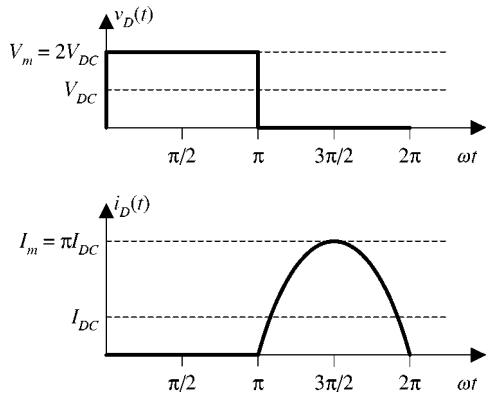


Fig. 1. Voltage and current waveforms of a class-F power amplifier.

This paper presents the study of a MOSFET amplifier in class-F operation, where the harmonics termination is optimally chosen to obtain high efficiency from a low-voltage low-gain operation. Based on the study, an amplifier was implemented in a standard 0.6-μm CMOS technology. Its design and comparison of experimental results on the tested prototype with simulations are presented.

II. Class-F Operation

Efficiency improvement in power amplifiers can be obtained by flattening either current or voltage waveforms or both [9]. This flattening is achieved by driving the active device into triode or cutoff regions. There are several ways to achieve the waveform flattening, which defines the different operating classes. The type of flattening is not only dependent on the device conditions, but also on the output load filtering.

A. Ideal Class-F Operation

Class-F operation was firstly defined when half-rectified current and square voltage waveforms at the active device output were present (Fig. 1) [10]. To accomplish this behavior, the active device has a bias point at the cutoff region and the output load must ensure the required spectrum for current and voltage. The current has a fundamental (first harmonic) and even harmonics, while the voltage has the fundamental and odd harmonics: *odd class-F* operation. Therefore, the load must present an open or short at odd or even harmonics, respectively.

The concept of class F is wider than stated above. By changing the load filter resonators in order to present an open circuit at even harmonics and a short circuit at odd harmonics, the waveforms would turn into an half-rectified voltage and square current, obtaining the dual topology of class-F: *even class-F* operation. Both types of class-F amplifiers lead theoretically to 100% efficiency. Since the two spectra are correlated only at the fundamental, no power is wasted in the load at higher order harmonics. Moreover, the active device presents a null voltage drop when the current is flowing, and when a voltage is present at its output port, the current is null.

B. Class-F with Real Loads and Ideal Active Device

In the previous description, a class-F power amplifier loaded with an infinite number of resonators was assumed. In the real world, filters have a finite order. The way this limitation affects a class-F power amplifier was studied by Raab [7]. He derived the harmonics magnitude required for flattening both voltage and current waveforms when the load presents a finite number of resonators in both types of class-F amplification.

When using a finite number of harmonics for shaping the voltage waveform, and assuming that the current is a half-rectified sine, odd class F leads to a higher efficiency than even class F. When the number of tuned harmonics increases, a higher improvement on efficiency of even class F is obtained. Tuning the voltage second harmonic and assuming a square wave current increases the efficiency from 63.7% to 84.9% (+21.2%), while the third harmonic tuning raises the efficiency from 78.5% to 88.4% (+9.9%). Tuning additional harmonics has little effect on efficiency either in odd or even modes. The fourth harmonic improves efficiency only 5.6%, while the fifth improves 3.6%.

In conclusion, considering only one harmonic in both class-F topologies, a high-efficiency improvement is obtained, leading to similar values. When tuning additionally to the fundamental the second or third harmonic, the optimum load $R_{\rm L}$, defined as the ratio between the first harmonics of the voltage and current waveforms, has the value of $(3/\pi)R_{\rm DC}$ and $(9/4\pi)R_{\rm DC}$, [7]. $R_{\rm DC}$ is the ratio between the average bias voltage and current $R_{\rm DC} = V_{\rm DC}/I_{\rm DC}$. In the following sections, we will refer to second harmonic peaking as "2H" (even class F with only one resonator) and third harmonic peaking as "3H" (odd class F with only one resonator).

C. Class-F 2H and 3H with an MOS Device

In this paper, for odd class F, the current is always assumed as a half-rectified sine, while the voltage contains first and third harmonics. In even class F, current is a square wave, and the voltage contains the first two harmonics.

In this section, a special emphasis is given to the use of an MOS transistor from a 0.6-μm CMOS standard technology with a low bias voltage (3 V). As shown in the previous section, tuning the second or third harmonic leads to similar amplifier efficiency. Besides the amplifier efficiency, parameters such as output power, gain, or PAE are also of vital importance in RF power-amplifier design. Therefore, the amplifier's performance for such parameters must be evaluated as well: the gain and efficiency of a CMOS monolithic power amplifier as a function of input power for both 2H and 3H topologies with the same output power are analyzed.

To study the amplifier behavior due to the voltage-controlled current source of the MOSFET model, the circuit is simulated at low frequency in order to neglect other model elements. The use of an nMOS device affects the desired output waveforms, mainly when driven into the triode region. Its ON resistance $R_{\rm ON}$ reduces the voltage swing and, therefore, the optimum load value. To obtain the same output power, the current has to increase to compensate the $V_{\rm DSON}$ voltage drop. Assuming for the MOSFET the low-frequency model, it is not possible to use the theoretical values obtained by Raab for ideal waveforms. For a better comparison, each power-amplifier topology uses the load for maximum output power, leading to the same power for both topologies. The simulations were performed with spectreRF,[1] which is an appropriate tool for one-tone strongly nonlinear circuits. The power-amplifier circuit is presented in Fig. 2.

The value of the MOS device gatewidth must be large enough to handle the required current and also to ensure a low dc output $I(V)$ curves knee voltage $V_{\rm DSS}$. On the other hand, a large gatewidth has associated large parasitic capacitance. An optimum value of 1200 μm for the gatewidth with a gate length of 0.6 μm, (the minimum allowed by the used process[2]) was found.

The bias for each topology must allow the desired current waveforms. For the 2H class F, the active device is biased at half the maximum expected current, resulting in a symmetrical waveform, which becomes a square wave when the input power is increased. For the 3H class F, the active device is biased near the cutoff region, resulting in a half-rectified drain–current waveform.

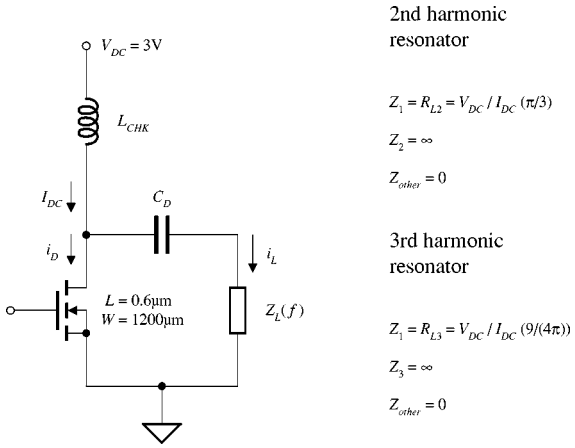


Fig. 2. Class-F power amplifier with simple resonator.

The output load value depends mainly on the dc current in the amplifier and on the MOSFET $R_{\rm ON}$ resistance. This situation is obtained when the amplifier is saturated as a way to avoid dependence of output power with input power. For 2H, no matter the input power value, the dc current remains constant, and so does the output load optimum value. However, for 3H, the dc current, as well as the output optimum load, depends on the input power. In order to have comparison criteria, we must obtain the same output power with both types of class-F amplifiers. The curves in Fig. 3(a) show an optimum load value of 21 Ω for 2H and 11 Ω for 3H, which lead to the same maximum output power for both operation conditions. However, increasing the output load to 22 and 12 Ω for 2H and 3H, respectively, improves the efficiency at the cost of a slight reduction on output power.

Fig. 3(b) shows the output power and efficiency as a function of input power. 2H class F presents higher output power and efficiency values for lower input power than class-F 3H. The 2H amplifier, which needs a lower gate drive voltage, has more than 6 dB of power gain than the 3H amplifier before the 1-dB compression point. The current flowing in the MOSFET in 3H case goes up to $\pi\ I_{\rm DC}$ and in 2H goes only up to $2\ I_{\rm DC}$. Accordingly, for the 3H case, a higher $V_{\rm DSON}$ is reached, and the current increase to compensate this voltage drop lowers the efficiency.

III. CMOS Power Amplifier

Based on the previous conclusions, a CMOS even class-F power amplifier for wireless communications ($P_{\rm out} = 23$ dBm @ $f = 1.9$ GHz) was designed, taking into account the low gain of MOS devices at the gigahertz range. The amplifier design is aimed to minimum gain reduction due to the optimization of other characteristics. In a first step, with the device operating at low frequency and a second harmonic tuning (2H class F), the predicted efficiency was 55% with a gain compression of 2.3 dB, which is much lower than the theoretical prediction by Raab [7]. This is due to the important effect of $R_{\rm DSON}$ on a low dc-bias amplifier. The amplifier was then evaluated at the desired frequency of 1.9 GHz and the entire circuit redesigned.

The technology used to implement the amplifier is a standard CMOS double-poly double-metal process. This process, like any other standard CMOS technology, allows the implementation of n-p MOS and lateral bipolar transistors and diodes as active components, and resistors and capacitors as passive components. Inductors are not standard components in CMOS.

[1]Cadence, version 4.4.1, San Jose, CA, 1997.

[2]Austria Micro Sistems (AMS) 0.6-μm CMOS design rules.

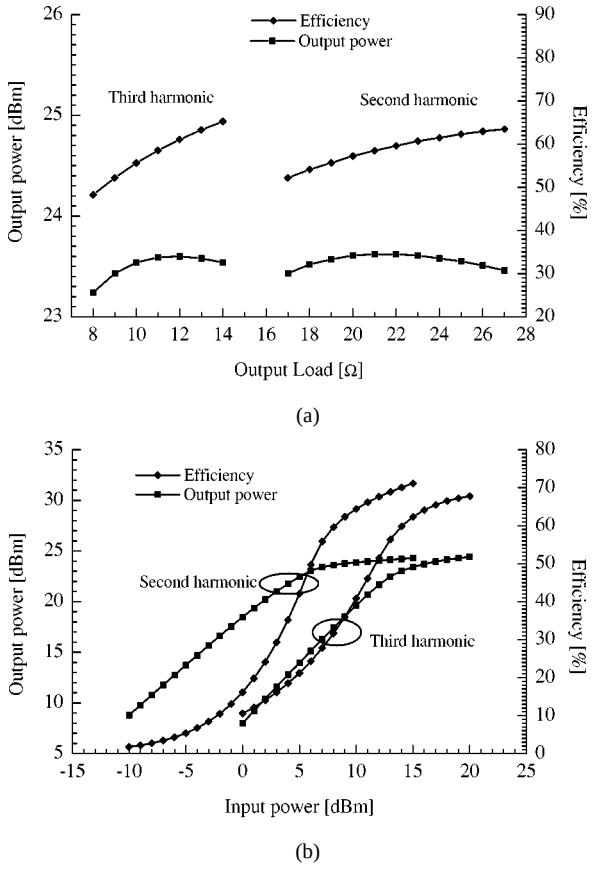


Fig. 3. Amplifier 2H and 3H output power and efficiency performance. (a) As a function of the output load. (b) As a function of the input power.

A. Power MOS Device Layout

This amplifier uses one MOS device with a gatewidth of 1200 μm and the minimum gate length of 0.6 μm, as in the low-frequency study (Section II-C). The total gatewidth is divided in a number of fingers optimized for high frequency and high current operation [11]. The current is limited by each drain finger strip width. In accordance, it must have as many fingers as possible. The poly used in a MOSFET gate presents a high resistance. Using several fingers decreases the total gate resistance. The optimum geometry found for the active device was 48 fingers with 25 μm each (50 $\times$ 110 μm^2 of silicon surface). Since a key tool for the proper design of highly nonlinear power amplifiers is the active device model, special attention was given to this subject. Due to the gate multifinger distributed structure, an equivalent lumped circuit was used to model the gate series resistor.

B. Output Matching Network

The most important block of this power amplifier is the output matching network. This network must convert the 50-Ω system impedance into the active device load, which maximizes output power at the first harmonic frequency, and has to present an open circuit at the second harmonic frequency and a short circuit at all other harmonics. This network is to be implemented with a standard CMOS process, with a limited type of components and values.

To implement resonators, we need inductors and capacitors. Capacitors can easily be obtained in CMOS between poly layers, which allow high capacitance per unit area. However, inductors suitable for this application are not easily available. It is possible to integrate spiral inductors in silicon substrates with Q-factors of 3$\sim$10 using multilevel spirals [12], high-resistive substrates [13], or both techniques. However, with these low-Q-factor inductors, series resistance is close to the optimum load value, leading to high losses. Another drawback of the monolithic spiral inductor is the chip area requirement (typically squares with 500 $\times$ 500 μm^2), which is high even when compared with the quite large MOS power device.

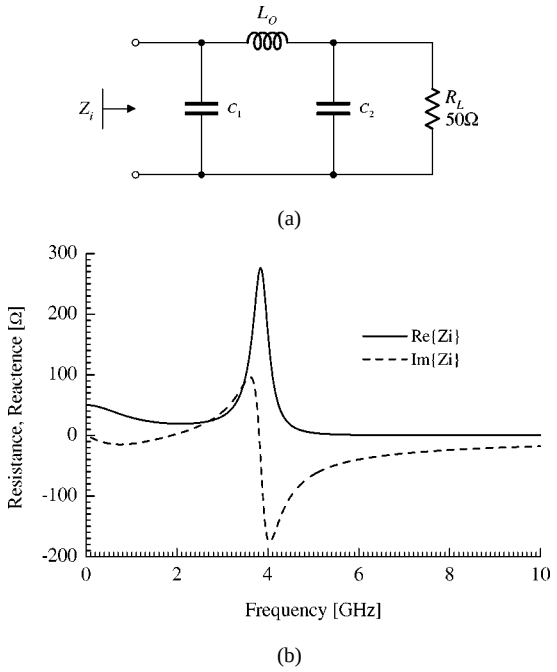


Fig. 4. Output matching network. (a) Circuit topology. (b) Impedance curves.

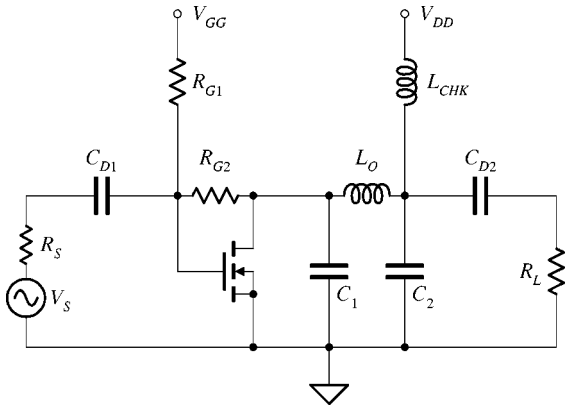


Fig. 5. Power amplifier circuit for 1.9 GHz.

The adopted solution to integrate inductors was to use bond-wire inductance, which is always needed for chip connection [11]. The bond wire has the advantage of an almost negligible series resistance. However, by using bond-wire inductance, the matching network topology is limited to the use of a series inductor, such as the matching network presented in Fig. 4(a). The addition of capacitors C_1 and C_2 provides the optimum termination for class F with only second harmonic tuning (Π low-pass filter).

Inductor L_O is a bond wire with a length that provides the required inductance. The wire used has an inductance of 0.7 nH/mm. Capacitor C_1 is an on-chip small poly-capacitor in parallel with the MOSFET output parasitic capacitance. Capacitor C_2 is an off-chip surface-mount device (SMD) capacitor.

The curve presented in Fig. 4(b) shows the input impedance of the Fig. 4(a) network. It can be noticed that all load requirements are accomplished. At the second harmonic, capacitor C_2 acts as a short circuit, and the MOSFET drain becomes loaded with the parallel reso-

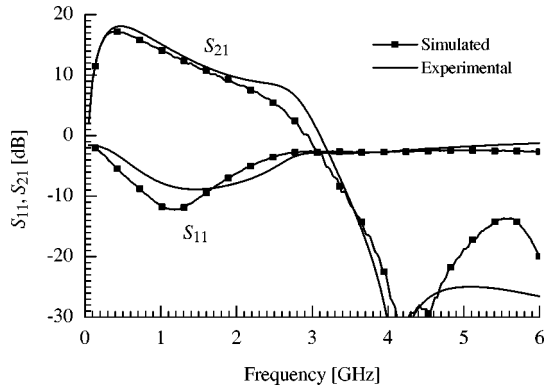
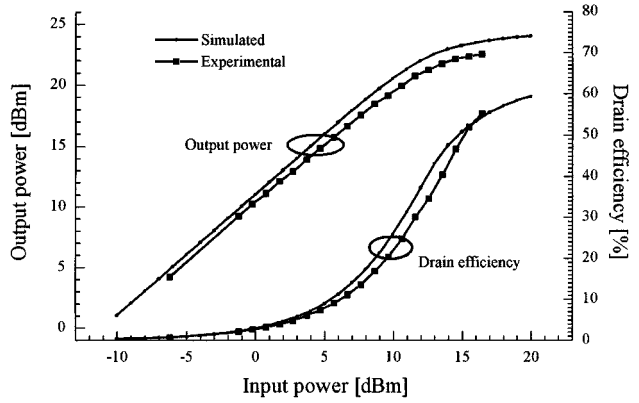
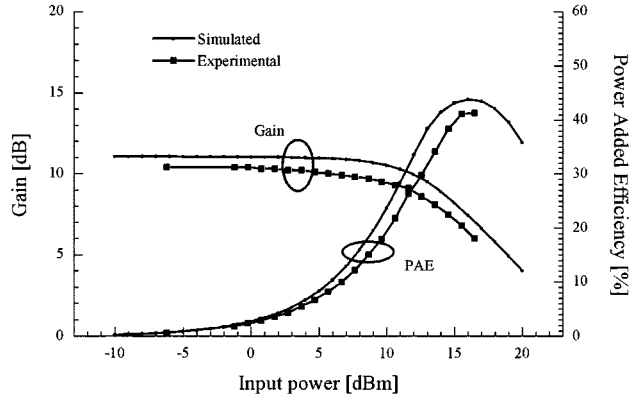


Fig. 6. Power amplifier S_{11}- and S_{21}-parameters.



(a)



(b)

Fig. 7. Power-amplifier large-signal performance. (a) Output power and drain efficiency. (b) Gain and PAE.

nance of C_1 and L_O. For higher frequencies, capacitor C_1 presents low impedance.

The complete amplifier circuit is presented in Fig. 5. Capacitors $C_{\rm D1}$ and $C_{\rm D2}$ are used for dc decoupling and $L_{\rm CHK}$ is used for drain bias. Resistor $R_{\rm G1}$ ensures the gate bias. In order to stabilize the MOSFET at lower frequencies, the feedback parallel resistor $R_{\rm G2}$ was introduced.

C. Power-Amplifier Performance

The simulations of the power amplifier were performed with SpectreRF. The small-signal characteristics are presented in Fig. 6 as S_{11}- and S_{22}-parameters. The amplifier shows an experimental gain of 9.5 dB and input return losses of -7 dB, which agrees with the simulations.

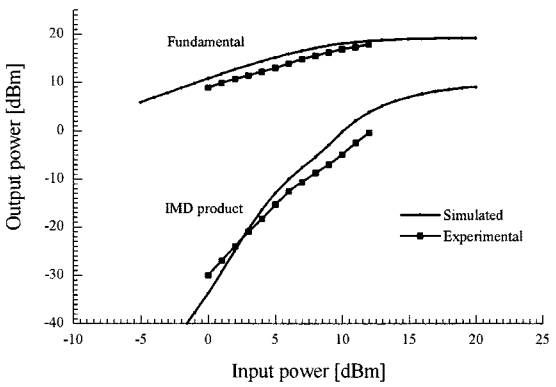


Fig. 8. Power amplifier IMD performance.

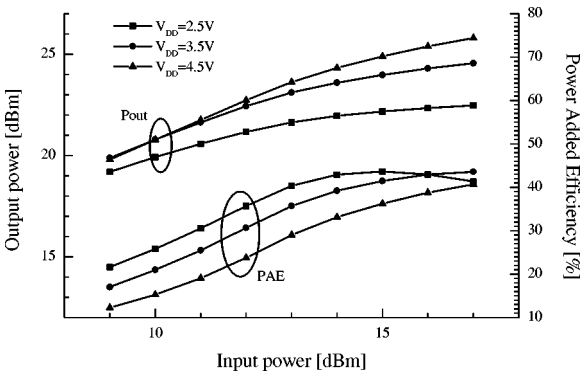


Fig. 9. Power-amplifier performance as a function of input power for several bias voltages.

The large-signal performance simulated and measured are presented in Fig. 7 for comparison purposes.

The amplifier was tested with a 3-V power supply and a 1.9-GHz drive signal, presenting a small-signal gain of 10.5 dB and a saturated output power $P_{\rm osat}$ of 22.8 dBm. The maximum value of PAE, i.e., 42%, was obtained for $P_{\rm out} = 22.5$ dBm. A good agreement with the predicted values can be noticed on small-signal and power measurements.

The second and third harmonic level was measured at -28.7 and -38.4 dBc for the maximum PAE condition. These values are close to the simulated, i.e., -30.4 and -40.1 dBc, respectively.

Intermodulation distortion was tested by applying two tones of 1.8 and 1.9 GHz at the amplifier input. The simulated and measured performance is shown in Fig. 8. The amplifier presents a distortion of 38.8 dBc for an input power of 0 dBm, leading to a third-order intermodulation intercept point (IIP3) of 19.5 dBm.

In order to evaluate the amplifier performance with different drain voltage bias, simulations were performed with $V_{\rm DD} = 2.5$ V, 3.5 V, and 4.5 V; however, with the optimum load for $V_{\rm DD} = 3$ V. Fig. 9 shows the output power and PAE evaluation for these drain bias conditions. An output power of 26 dBm is possible when using a 4.5-V power supply. Using 2.5 V, an output power of 22 dBm with a PAE of 43% is obtained with an input power of 15 dBm. For these bias conditions, we noticed an almost constant PAE when the output is close to saturation.

IV. Conclusions

A theoretical study of class-F power amplifiers operation with a low-frequency active device model has been presented in this paper, showing that tuning the second harmonic frequency (even class F) has

advantages over tuning the third harmonic (odd class F), i.e., higher efficiency and output power for the same drive level and higher gain.

Accordingly, an integrated even class-F CMOS power amplifier operating at 1.9 GHz with 3-V power supply was designed and tested. The amplifier uses a monolithic microwave integrated circuit (MMIC) with the power transistor, a stabilizing resistor, and part of the bias network. The output filter, for a proper harmonic treatment, uses the bond wire as a high-Q inductor. The results show a good agreement with experiments, not only for a small signal, but also for output power saturation ($P_{\rm osat} = 22.8$ dBm) and PAE (PAE $= 42\%$) with a large signal.

The measured performance shows the possibility of designing low-voltage power amplifiers in a standard CMOS technology for several wireless systems specifications, such as digitial enhanced cordless telephone (DECT) or future generations such as Universal Mobile Telecommunications System (UMTS) standard-based systems. In fact, when shorter channel length technologies become competitive in cost, power amplifiers for higher frequencies can be designed using the technique described in this paper.

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